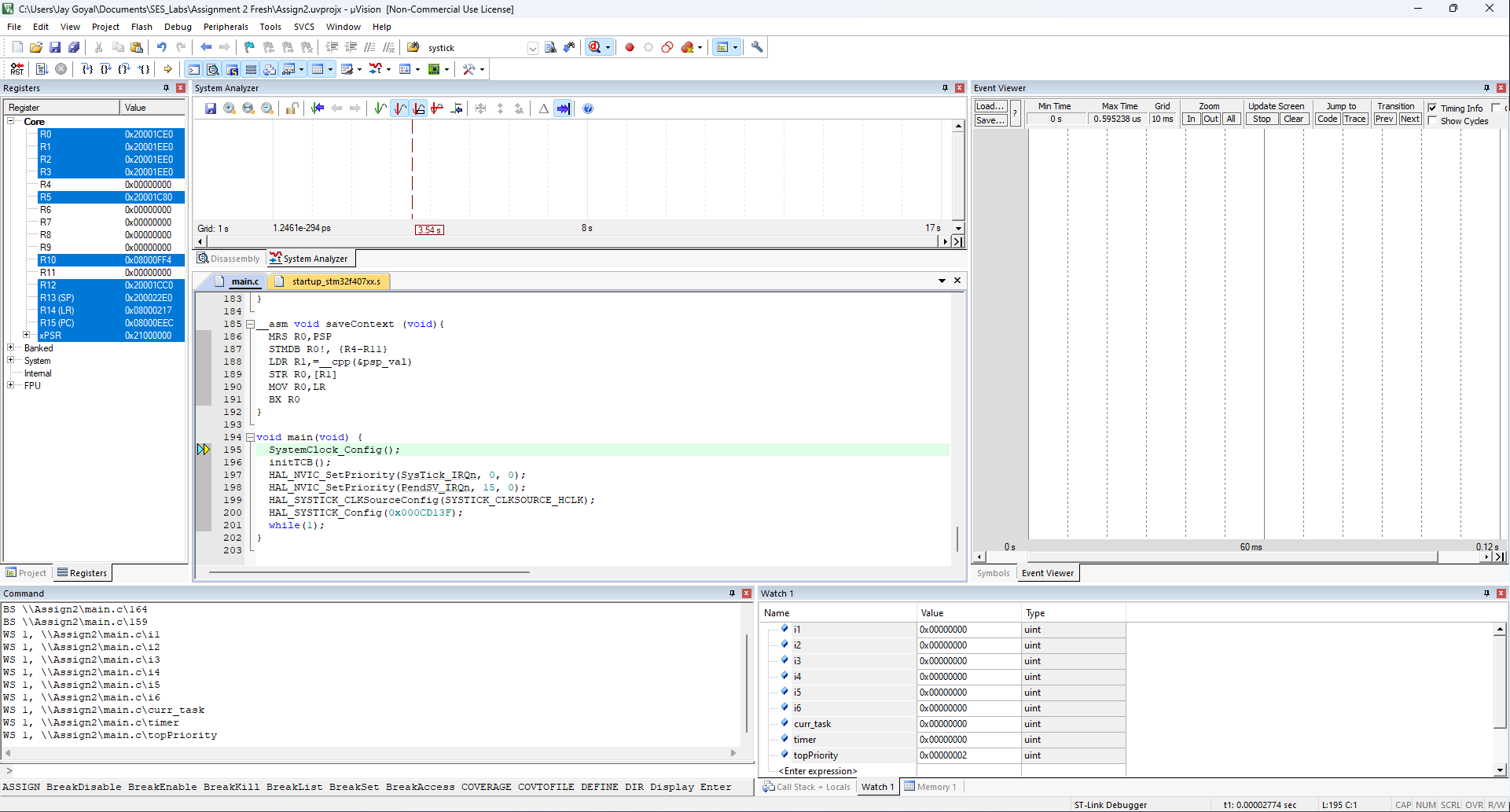
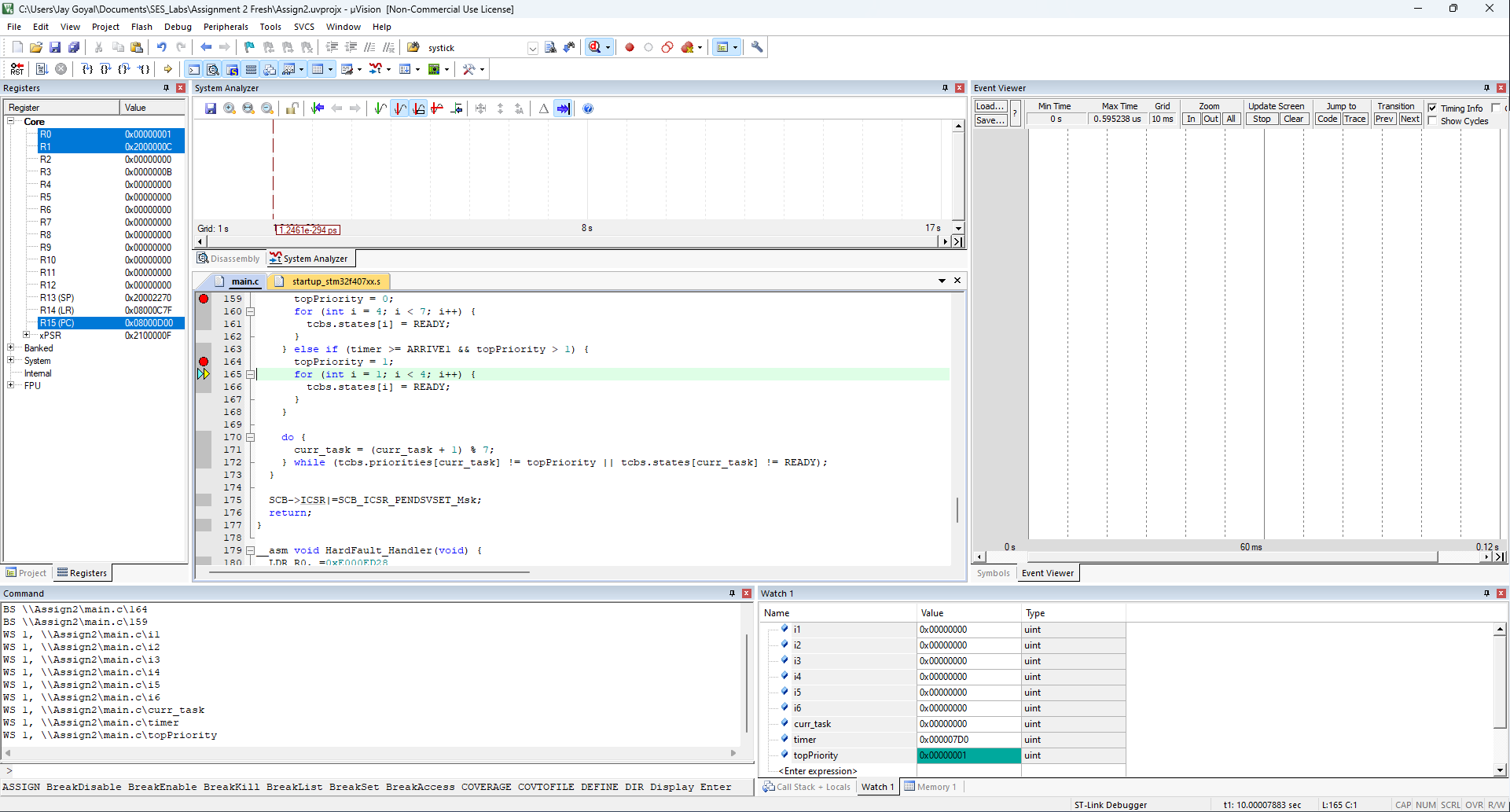
This is the description of the Software for Embedded Systems Assignment 2.

For the code, the scheduling example uploaded on Nalanda served as an inspiration. The clock configuration code was taken directly from the example to configure the clock at 168MHz. The results are as follows:

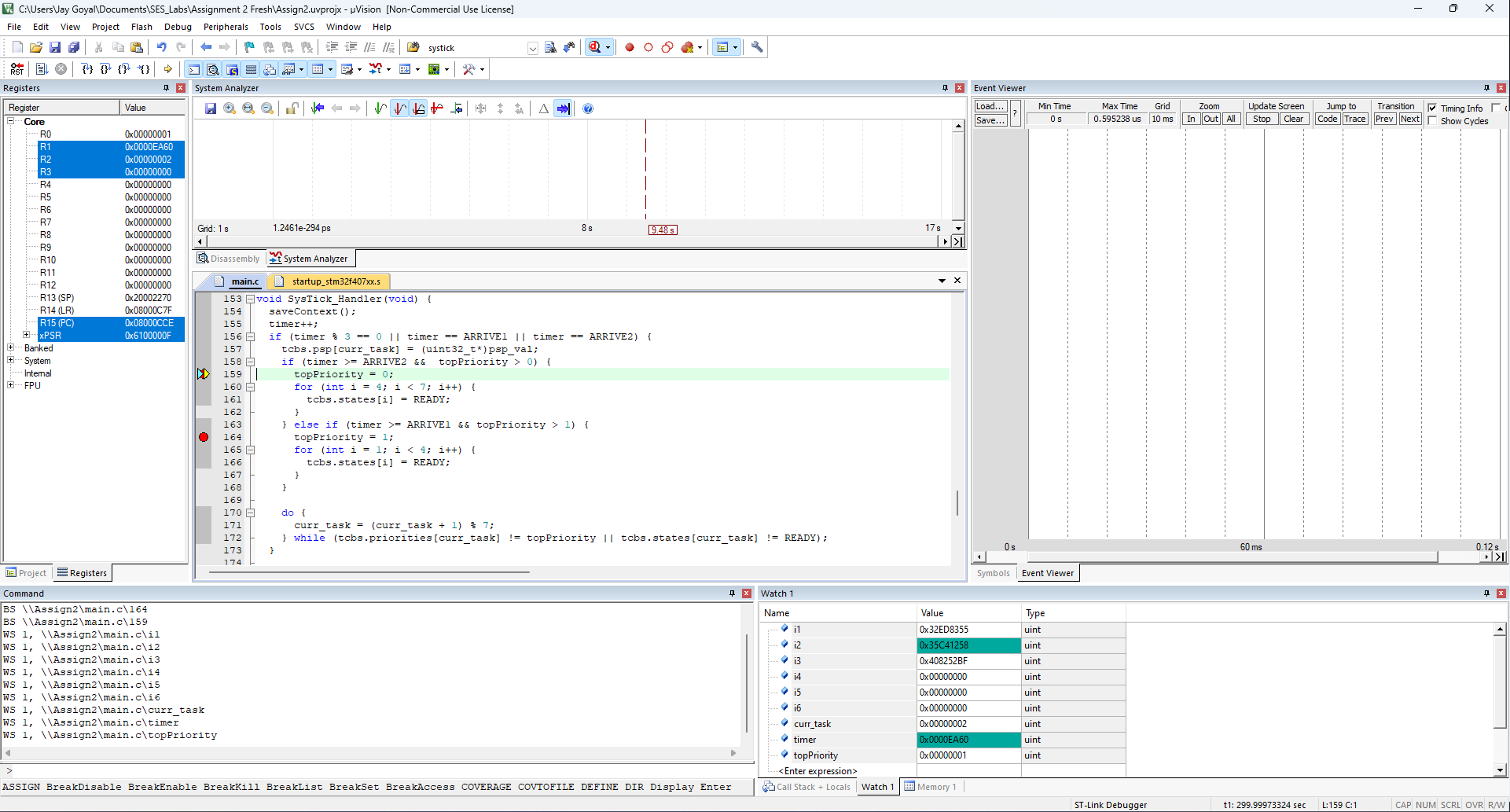
1. At t=0, all the variables are 0, with the priority of the running tasks set to 2, the lowest possible level, that given to the idle task (handled within the main function).



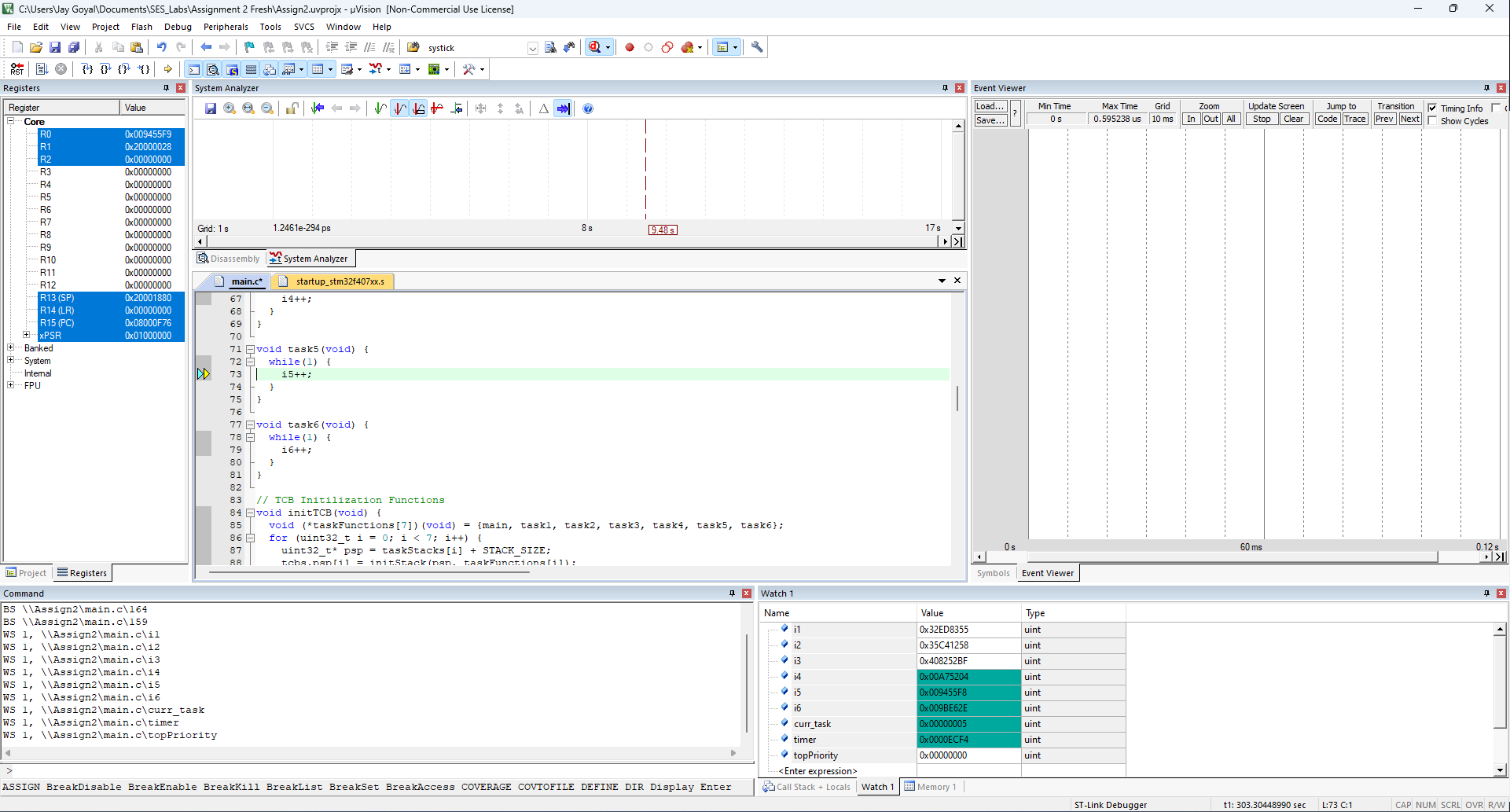
1. At t=10s, tasks 1, 2 and 3 are put into the ready state using the SysTick ISR. This makes these tasks run in a round robin fashion. At this stage, the idle task stops running because it has a lower priority.



1. At t=300s, tasks 4, 5 and 6 are put into the ready state as before. This causes tasks 1, 2 and 3 to stop and tasks 4, 5 and 6 are executed in a round robin fashion. The execution of the first 3 tasks can also be seen as the variables i1, i2 and i3 are incremented. We can also see that i4, i5 and i6 are 0, indicating that tasks 4, 5 and 6 were not executed until this point.



1. At t>300s, we see that i4, i5 and i6 are changing while i1, i2 and i3 remain the same, indicative of the fact that tasks 1, 2 and 3 stop running.



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